PATENT ABSTRACTS OF JAPAN

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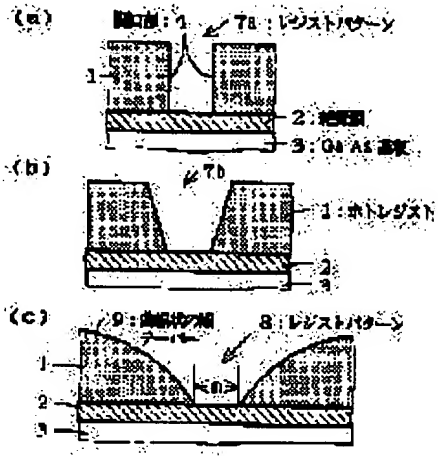
(54) MANUFATURE OF SEMICONDUCTOR DEVICE

(57)Abstract:
PURPOSE: To suppress sputtering of etching substance on the side wall of a resist aperture part, and to prevent the growth of a modified substance film consisting of a mixture by a method wherein the side wall of the aperture part of a resist pattern is deformed into a curved forward tapered shape by reflowing the resist film by heating.
CONSTITUTION: An SiO2 film 2 is deposited on a GaAs substrate 3, and a resist pattern 7a, having an aperture 4 is formed thereon. Then, a resist 1 is heated up, and when its reflow is started, the upper part of the resist moves to the spreading direction on the aperture part 4 by the action of surface tention, the size (m) of the aperture bottom part is unchanged, the side wall of the aperture is turned to semicylindrical curve 9, and the final resist pattern 8 is formed in a stable manner. As a result, the sputtering of the substrate to be etched on the side wall of the resist aperture part is suppressed, and the growth of the modified substance, consisting of a mixture, can be prevented.



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CLAIMS

[Claim(s)]

[Claim 1] The manufacture method of the semiconductor device characterized by including the process made to deform the opening side attachment wall of the aforementioned resist pattern into a curve-like order taper by heated and carrying out a reflow of this resist film after developing the photoresist film which exposed the pattern.

[Claim 2] To the photoresist film after the aforementioned development, it is O2. The manufacture method of a semiconductor device including the process made to deform the opening side attachment wall of the aforementioned resist pattern into a curve-like order taper by heated and carrying out a reflow of this resist film after performing plasma treatment and forming a transformation layer in this photoresist film front face according to claim 1.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] this invention is used for formation of the resist pattern for imprinting the detailed pattern especially in lithography technology about the manufacture method of a semiconductor device.
[0002]
[Description of the Prior Art] It explains taking the case of the process which uses a resist as a mask as 1st conventional example which imprints a detailed pattern at the insulator layer formed on the semiconductor substrate, and imprints a detailed opening pattern.
[0003] In using a resist etc. as a mask, carrying out dry etching of the insulator layer and imprinting a pattern conventionally, the opening width-of-face size of a resist used as a mask has that ideal to which it is a size near a design value, and the side attachment wall has accomplished the taper a perpendicular and a little mostly, and the resist pattern (resist film with which the figure drawn on the resist in the opening slot or the figure was drawn) is used for it, and it is **********ing the target ground insulator layer. Drawing 8 and drawing 9 are the cross sections showing the conventional manufacturing process when performing regist patterning and **********ing a ground insulator layer.
[0004] drawing 8 (a) -- Ga As Si O2 formed in the substrate 3 Or Si 3N4 etc. -- on an insulator layer 2, a resist 1 is applied and it has opening 4 It is drawing in which opening pattern (figure on which the NUKIPA turn was drawn in call opening slot) 6a of 0.1-micrometer level was formed. It further overly turned minutely from submicron one. In the size level of 0.1 micrometers or less, in the present condition, an electron beam is used and regist patterning is performed. In this case, the opening side attachment wall of the resist pattern after development serves as a back taper configuration in response to the influence of a perpendicular or the back squitter of an electron beam. Next, in this drawing (b), if the ground layers (Si O2 film etc.) 2 are **********ed by (CF4+O2) / (CF4+H2) etc. using the resist pattern of the above-mentioned configuration, processing to which the side attachment wall rose steeply in the perpendicular mostly is possible. However, in this case, since the width of face of opening is narrow, in the usual dry etching, power matter 5a which it **********s efficiently and scatters (spatter) will surely adhere to an opening side attachment wall. Therefore, it is the resist after original etching is completed O2 When it exfoliates in Usher etc., as shown in drawing 9 (a), the resist of the shape of a thin film, the matter with which it **********ed, and the transformation matter film 5 which consists of mixture of etching gas material further will remain. In addition, a sign 6 is the opening pattern imprinted by the insulator layer 2. For this reason, as shown in this drawing (b), the addition of the wet processing which removes the transformation matter film 5 by the ammonium fluoride is needed.
[0005] on the other hand, the design of an element -- general -- the width-of-face size (it is only described as a pattern size below) of opening of a pattern -- size -- various things are intermingled Since, as for etching gas, a pattern size cannot enter easily like a narrow, an etching rate will become late. therefore -- 0.1 micrometers if the pattern of about 1-micrometer variation of tolerance is intermingled -- an etching rate -- differing -- for example, -- If the amount of etching of 0.1-micrometer field is made into a proper value, over etching will be carried out in 1micrometer field.
[0006] Next, as 2nd conventional example which imprints a detailed pattern, it is Ga As. The example which forms T type (mushroom type) gate pattern used by devices (HEMT etc.) is explained. Drawing 10 is the cross section showing the manufacturing process of T type gate pattern by the conventional bilayer resist method. It sets to this drawing (a) and is Ga As. On a substrate 3, the lower layer resist film 12 which has the opening pattern 15 (for example, pattern size 0.2micrometer) is formed, the upper resist film 13 of T type gate pattern crowning is formed by the resist which next does not have compatibility, and the gate metal 14 is deposited. Next, a resist is removed by the lift-off method, and as shown in this drawing (b), T type gate pattern 16 is formed.
[0007] About the bilayer resist process method, gate length is determined with the pattern size of the opening pattern 15 formed by the lower layer resist film 12. Therefore, as an opening pattern 15, the precision of the width-of-face size of opening is good, and what has the still more nearly perpendicular resist side attachment wall of opening is desirable.
[0008] However, when it carries out and the opening pattern 15 deposits gate metal at the following process in the above-mentioned configuration, it becomes easy to generate a nest in gate metal from causes, like step KAPAREJI (the covering state of the film in the detailed level difference section in the front face of semiconductor device thin films, such as step coverage and LSI) becomes bad.
[0009] Next, as 3rd conventional example which imprints a detailed pattern, the formation method of T type gate pattern which makes the aforementioned T type gate pattern another conventional technology, and makes an insulator layer a spacer is explained. Drawing 11 is the cross section showing this manufacturing process. this drawing (a) -- setting -- Ga As Si O2 of thickness 100 nm which serves as a spacer on a substrate 3 - 200 nm etc. -- an insulator layer 21 is deposited, the resist pattern 22 is formed on it, next dry etching of the insulator layer 21 is carried out, and opening 25 is formed Next, as shown in this drawing (b), the gate metal 24 is deposited, as shown in this drawing (c), a resist is removed by the lift-off method and T type gate pattern 26 is formed.
[0010] The size of a contact portion with the substrate of the above-mentioned T type gate pattern is determined with the opening size of the opening 25 of an insulator layer 21. In formation of a detailed pattern, the etching method has changed to dry etching from wet etching as a recent trend. therefore, Si O2 etc. -- if an insulator layer **********s, the side attachment wall of opening is formed in the almost perpendicular configuration However, a spacer is the thickness about 100nm - 200 nm, and does not become not much large [an aspect ratio]. Therefore, the step coverage when depositing gate metal is enough, and generating of a nest is not seen.
[0011] however, an etching of a detailed pattern sake -- CF4 required for dry etching NF3 etc. -- gas cannot go into opening easily, etching

rates with a large pattern (for example, 1-micrometer level) differ, and it worries about the injury by over etching
[0012]
[Problem(s) to be Solved by the Invention] When using a resist as a mask and imprinting a detailed opening pattern to a ground insulator layer like the aforementioned 1st conventional example (refer to drawing 8 and drawing 9), a pattern size When it turns into 0.1-micrometer level grade minutely, the ground insulator layer matter with which it **********s carries out a spatter, and adheres to the side attachment wall of resist mask opening, the transformation matter film with which after resist mask removal consists of mixture remains, and excessive processing is needed in order to remove this. if it becomes a detailed size on the other hand -- etching gas -- opening -- entering -- hard -- becoming -- a pattern size -- for example, -- 1 micrometer and other large patterns differ from an etching rate, and there is a fear of receiving an injury.
[0013] Moreover, the technical problem that the step coverage of resist opening is bad like the aforementioned 2nd conventional example when forming T type gate pattern on a substrate by the lift-off method of a bilayer resist (refer to drawing 10), and a nest occurs in gate metal occurs.

[0014] Moreover, although it loses the technical problem of a step coverage in making an insulator into a spacer and forming T type gate pattern on a substrate by the lift-off method like the aforementioned 3rd conventional example (refer to drawing 11), by the size of a pattern size, etching rates differ, a large pattern serves as over etching, and there is a fear of receiving an injury.
[0015] It is what was made in order that this invention might solve the above-mentioned technical problem when imprinting a detailed pattern. the 1st purpose It presses down that the spatter of the matter with which it **********s is carried out to the side attachment wall of resist opening in case an opening pattern is formed in a ground insulator layer etc. It makes it possible to prevent growth of the transformation matter film which consists of mixture. the 2nd purpose Etching gas is sent as much as possible also into opening of a detailed pattern. It is offering the manufacture method of the semiconductor device which it makes it possible to ********** at the rate near the etching rate of a large pattern size, and the 3rd purpose's improves a step coverage at the time of deposition of gate metal etc., and can prevent generating of a nest.
[0016]
[Means for Solving the Problem] After the manufacture method of the semiconductor device concerning the claim 1 of this invention develops the photoresist film which exposed the pattern, it is characterized by including the process made to deform the opening side attachment wall of the aforementioned resist pattern into a curve-like order taper (that to which a resist side attachment wall has the tilt angle of 90 degrees or less in a ground layer principal plane) by heating and carrying out a reflow of this resist film.
[0017] Moreover, the manufacture method of the semiconductor device concerning the claim 2 of this invention is O2 to the photoresist film after the aforementioned development. After performing plasma treatment and forming a transformation layer in this photoresist film front face, it is the manufacture method of a semiconductor device including the process made to deform the opening side attachment wall of the aforementioned resist pattern into a curve-like order taper according to claim 1 by heating and carrying out a reflow of this resist film.
[0018]
[Function] Generally the resist after development performs a postbake, and a developer is evaporated or it is made to harden it to some extent by heating for the following process. however, by the manufacture method concerning the claim 1 of this invention If the postbake temperature of the resist pattern after development is raised to near the glass transition temperature of a resist higher than before A reflow starts and the rough edge of the character of the shoulder of opening is rounded off with an operation of surface tension. It moves in the direction in which it is roundish and the resist upper part spreads, and finally the size of a contact portion with a ground is not changed, but the opening upper part spreads, and an opening side attachment wall serves as a boiled-fish-paste-like order taper, and is stabilized (refer to drawing 1 (c)).
[0019] The insulator layer matter with which it will carry out the spatter of the boiled-fish-paste-like resist pattern by etching if such an opening side attachment wall **********s a ground insulator layer as for example, a mask for etching, and it adheres to an opening side attachment wall decreases in number sharply, the adhering transformation matter film is very thin, and it is O2 of the following process. It is completely removed with a resist by Usher. Moreover, in opening of such a configuration, sending of etching gas also becomes easy and the etching rate can make it the value near the etching rate of the opening pattern of a large size. Moreover, if the gate pattern by the lift-off method is formed by the resist pattern with opening of such a configuration, the step coverage in an opening shoulder will improve sharply.
[0020] The manufacture method concerning the claim 2 of this invention is O2 to the resist pattern after development. Plasma is emitted, and after making it change to the matter which cannot solve the surface layer of a resist easily chemically, the same manufacture method as the above-mentioned claim 1 is applied.
[0021] detailed-izing -- progressing -- a pattern size -- for example, -- If it becomes thin below at 0.1-micrometer level, when a reflow of the resist film after development will be heated and carried out, opening may be closed conversely. By the manufacture method of a claim 2, the transformation layer which is hard to solve into a resist front face is formed, and it prevents that opening is closed. That is, the transformation layer of a resist film front face carries out the operation which prevents that the resist opening side attachment wall which counters carries out approach contact mutually by the reflow, and plugs up opening.
[0022]
[Example] First, by heating and carrying out a reflow of the photoresist film after development explains the process made to deform the opening side attachment wall of a resist pattern into a curve-like order taper with reference to drawing 1 . This drawing (a) is Ga As. It is Si O2 on a substrate 3. It is the cross section which deposited the film 2 (less than [thickness 500nm]), and formed on it resist pattern (it may be called opening pattern or NUKIPA turn) 7a which has opening 4. Next, if a resist 1 is heated and it raises to near the glass transition temperature of a resist, a reflow will start. If a reflow starts as shown in this drawing (b), it will move in the direction in which the resist upper part spreads in opening 4 by operation of surface tension. Sign 7b expresses the resist pattern which began to spread. Finally, as shown in this drawing (c), the size of a contact portion with the ground layer 2 is not changed, namely, the size m of an opening pars basilaris ossis occipitalis is not changed, but it is [a side attachment wall forms the boiled-fish-paste-like curve 9, and] stable [size]. A sign 8 expresses a final resist pattern. This configuration It can form also with a pattern size with a level of 0.1 micrometers or less. It is presumed for force, such as a self-weight of the surface tension of the resist which the photoresist film 1 has been [the configuration] near a glass transition temperature in the state of a reflow, the statical friction force between this resist and a ground layer (boundary tension), and a resist film, to balance.
[0023] this invention is applied mainly to a detailed pattern imprint, and is considered that the thickness of the etched layer of a ground has an effect in etching of the thin film below 500 nm.
[0024] Moreover, Ga As At elements, such as a device, especially HEMT, it is Ga As constitutionally. About dozens of nm needs to ********** beforehand a part for the contact surface of a substrate and a gate electrode by recess etching. Since this process is needed and gate

formation also forms gate metal by the lift off using a resist pattern, application of this invention is desirable.
[0025] Next, the 1st example which applied the claim 1 of this invention to the aforementioned 1st conventional example is explained with reference to drawing 2 and drawing 3 . it is shown in drawing 2 (a) -- as -- Ga As Si O2 deposited on the substrate 3 Or Si 3N4 etc. -- insulator layer 2 top Resist pattern 7a of 0.1-micrometer level is formed. At this example, it heat-treats at . resist development back which used PMMA (polymethylmethacrylate), and ZEP and Nippon Zeon for the resist 1, and the temperature of 100 degree C - 150 degrees C. A resist reflow begins, and heat-treatment is ended when a reflow is stable. As shown in drawing 2 (b), the resist pattern 8 which the side attachment wall transformed into the curve-like order taper 9 is obtained. Next, it is the ground insulator layer 2 CF4+H2 and CF4+O2 Using gas, as shown in drawing 3 (a), it **********ed by dry etching. They are after etching and a resist 1 O2 Ashing (remove a photoresist according to ashing in oxygen plasma) removes, as shown in drawing 3 (b). Although the resist pattern 8 had the curve-like order taper 9 in the above-mentioned example, in the ground thickness below 500 nm, the size conversion difference by the taper at the time of etching was not large. In addition, a size conversion difference is the width of face w1 of opening shown in drawing 2 (a), and the width of face w2 of the opening pars basilaris ossis occipitalis of the ground layer 2 shown in drawing 3 (b). It is a difference. Moreover, in order that a taper might attach a little the side attachment wall of the opening pattern 6 imprinted by the insulator layer 2, its coverage when depositing gate metal was also good.
[0026] in the above-mentioned example, although the opening side attachment wall of a resist pattern was made to deform into a curve-like order taper, a size conversion difference is also pressed down to the minimum, without the taper being imprinted by the ground film -- the opening pattern of 0.1micrometer level was able to be formed
[0027] It compares with the conventional technology, it is sharply thin, and the transformation matter film which grew up to be a resist opening side attachment wall by the spatter is O2 further on the occasion of the dry etching of the ground insulator layer 2 shown in drawing 3 (a). Since sputter etching is repeated and it is efficiently removed on the resist front face one by one with this resist configuration in ashing, it is O2. It became possible to remove the resist which contains a transformation matter film simply by ashing. Moreover, with the conventional technology of a perpendicular or a back taper configuration, although the opening side attachment wall of a resist pattern had produced the difference in the etching rate by the size of a pattern size, it was also able to make the difference small a little by using an opening side attachment wall as a curve-like order taper.
[0028] Next, the 2nd example (the lift-off method of a bilayer resist) which applied the claim 2 of this invention to the aforementioned 2nd conventional example is explained with reference to drawing 4 and drawing 5 . As shown in drawing 4 (a), it is Ga As about a positive resist 41. After using an application, a stepper, and an electron beam machine on a substrate 3 and drawing a pattern, negatives are developed and resist pattern 47a is formed. Next, O2 used for the usual resist ablation processing A plasma ashing device is used and it is O2 with about 50W] power. Flow rate 150 cc/min Processing is performed for 30 seconds, and as shown in this drawing (b), it is made the transformation layer 42 which cannot solve a resist surface layer easily chemically. 120 **-160 ** and 1 a part -2 a part -- a grade -- the substrate 3 was heated on the hot plate, a reflow of the photoresist 41 was carried out, and as shown in this drawing (c), the resist opening side attachment wall currently formed perpendicularly was formed in the order taper of about 60 degrees with 0 micrometer of size conversion differences at the base of opening [next,] A sign 48 expresses a lower layer resist pattern with this order taper side attachment wall 49. Next, as shown in drawing 5 (a), the upper resist pattern 46 of T type gate crowning is formed by the resist 43 without compatibility, and the gate metal 44 is deposited. As shown in this drawing (b), a resist is removed by the lift-off method and gate 44a is formed.
[0029] Since the curve-like order taper side attachment wall 49 is made to deform the side attachment wall of resist pattern 47a of the lower layer resist 41 of the 2nd example of the above as shown in drawing 4 (c), the step coverage of the gate metal 44 is good, and a nest does not generate it. Moreover, it is mitigated sharply, the phenomenon in which the side attachment wall which counters mutually [opening] to the resist pattern formation into which the opening size turned minutely more since a reflow is carried out after considering as the transformation layer 42 which cannot solve the photoresist surface layer after development into this example easily contacts, and a pattern is closed can also form the order taper of about 60 degrees as mentioned above, and it is an opening pars-basilaris-ossis-occipitalis size in that case. It was less than ten percent of change.
[0030] Next, the 3rd example (the lift-off method which makes an insulator a spacer) which applied the claim 2 of this invention to the aforementioned 3rd conventional example is explained with reference to drawing 6 . it is shown in this drawing (a) -- as -- Ga As Si O2 which accumulates on a substrate 3 and serves as a spacer etc. -- the O2 [same after forming resist pattern 57a which consists of a positive resist 51 on an insulator layer 52] as the 2nd example of the above Plasma treatment is performed and the transformation layer 54 is formed in a resist film front face. Next, as shown in this drawing (b), an opening side attachment wall is used as the curve-like order taper side attachment wall 59 by heating and carrying out a reflow of the resist 51. Next, as shown in this drawing (c), the opening pattern 56 of an insulator layer is formed by processing an insulator layer 52 by dry etching, such as RIE, and removing a resist.
[0031] By this example, since it is a curve-like order taper side attachment wall, an etching rate becomes early and turns into an etching rate of a pattern with a large pattern size from the case where the side attachment wall of a resist pattern is the perpendicular former closely. That is, the difference of the etching rate by the size of a pattern size can be decreased. Moreover, by forming the transformation layer 54, it compares with the manufacture method concerning a claim 1, and a pattern size can also form a narrow pattern more, without closing opening.
[0032] In order to make the configuration of the opening side attachment wall of a resist pattern into an order taper configuration, there is also the method of light exposure being insufficient and exposing so that it may become thinner than a design size (refer to drawing 7).
[0033]
[Effect of the Invention] it explained in full detail until now -- as -- this invention -- the photoresist film after development -- immediately -- or after forming a transformation layer in a photoresist film front face, a reflow is carried out and the opening side attachment wall of a resist pattern is made to deform into a curve-like order taper By this invention, in case an opening pattern is formed in an insulator layer etc., for example, the matter with which it **********s It presses down that a spatter is carried out to the side attachment wall of resist opening, and it becomes possible to prevent growth of the transformation matter film which consists of mixture. Moreover, etching gas is sent as much as possible also into opening of a detailed pattern. It could ********** at the rate near the etching rate of a large pattern size, the step coverage at the time of depositing gate metal etc. on a resist pattern further was able to be improved, and the manufacture method of the semiconductor device which can prevent generating of a nest was able to be offered.

[Translation done.]

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TECHNICAL FIELD

[Industrial Application] this invention is used for formation of the resist pattern for imprinting the detailed pattern especially in lithography technology about the manufacture method of a semiconductor device.

[Translation done.]

PRIOR ART

[Description of the Prior Art] It explains taking the case of the process which uses a resist as a mask as 1st conventional example which imprints a detailed pattern at the insulator layer formed on the semiconductor substrate, and imprints a detailed opening pattern.
[0003] In using a resist etc. as a mask, carrying out dry etching of the insulator layer and imprinting a pattern conventionally, the opening width-of-face size of a resist used as a mask has that ideal to which it is a size near a design value, and the side attachment wall has accomplished the taper a perpendicular and a little mostly, and the resist pattern (resist film with which the figure drawn on the resist in the opening slot or the figure was drawn) is used for it, and it is **********ing the target ground insulator layer. Drawing 8 and drawing 9 are the cross sections showing the conventional manufacturing process when performing regist patterning and **********ing a ground insulator layer.
[0004] drawing 8 (a) -- Ga As Si O2 formed in the substrate 3 Or Si 3N4 etc. -- on an insulator layer 2, a resist 1 is applied and it has opening 4 It is drawing in which opening pattern (figure on which the NUKIPA turn was drawn in call opening slot) 6a of 0.1-micrometer level was formed. It further overly turned minutely from submicron one. In the size level of 0.1 micrometers or less, in the present condition, an electron beam is used and regist patterning is performed. In this case, the opening side attachment wall of the resist pattern after development serves as a back taper configuration in response to the influence of a perpendicular or the back squitter of an electron beam. Next, in this drawing (b), if the ground layers (Si O2 film etc.) 2 are **********ed by (CF4+O2) / (CF4+H2) etc. using the resist pattern of the above-mentioned configuration, processing to which the side attachment wall rose steeply in the perpendicular mostly is possible. However, in this case, since the width of face of opening is narrow, in the usual dry etching, power matter 5a which it **********s efficiently and scatters (spatter) will surely adhere to an opening side attachment wall. Therefore, it is the resist after original etching is completed O2 When it exfoliates in Usher etc., as shown in drawing 9 (a), the resist of the shape of a thin film, the matter with which it **********ed, and the transformation matter film 5 which consists of mixture of etching gas material further will remain. In addition, a sign 6 is the opening pattern imprinted by the insulator layer 2. For this reason, as shown in this drawing (b), the addition of the wet processing which removes the transformation matter film 5 by the ammonium fluoride is needed.
[0005] on the other hand, the design of an element -- general -- the width-of-face size (it is only described as a pattern size below) of opening of a pattern -- size -- various things are intermingled Since, as for etching gas, a pattern size cannot enter easily like a narrow, an etching rate will become late. therefore -- 0.1 micrometers if the pattern of about 1-micrometer variation of tolerance is intermingled -- an etching rate -- differing -- for example, -- If the amount of etching of 0.1-micrometer field is made into a proper value, over etching will be carried out in 1micrometer field.
[0006] Next, as 2nd conventional example which imprints a detailed pattern, it is Ga As. The example which forms T type (mushroom type) gate pattern used by devices (HEMT etc.) is explained. Drawing 10 is the cross section showing the manufacturing process of T type gate pattern by the conventional bilayer resist method. It sets to this drawing (a) and is Ga As. On a substrate 3, the lower layer resist film 12 which has the opening pattern 15 (for example, pattern size 0.2micrometer) is formed, the upper resist film 13 of T type gate pattern crowning is formed by the resist which next does not have compatibility, and the gate metal 14 is deposited. Next, a resist is removed by the lift-off method, and as shown in this drawing (b), T type gate pattern 16 is formed.
[0007] About the bilayer resist process method, gate length is determined with the pattern size of the opening pattern 15 formed by the lower layer resist film 12. Therefore, as an opening pattern 15, the precision of the width-of-face size of opening is good, and what has the still more nearly perpendicular resist side attachment wall of opening is desirable.
[0008] However, when it carries out and the opening pattern 15 deposits gate metal at the following process in the above-mentioned configuration, it becomes easy to generate a nest in gate metal from causes, like step KAPAREJI (the covering state of the film in the detailed level difference section in the front face of semiconductor device thin films, such as step coverage and LSI) becomes bad.
[0009] Next, as 3rd conventional example which imprints a detailed pattern, the formation method of T type gate pattern which makes the aforementioned T type gate pattern another conventional technology, and makes an insulator layer a spacer is explained. Drawing 11 is the cross section showing this manufacturing process. this drawing (a) -- setting -- Ga As Si O2 of thickness 100 nm which serves as a spacer on a substrate 3 - 200 nm etc. -- an insulator layer 21 is deposited, the resist pattern 22 is formed on it, next dry etching of the insulator layer 21 is carried out, and opening 25 is formed Next, as shown in this drawing (b), the gate metal 24 is deposited, as shown in this drawing (c), a resist is removed by the lift-off method and T type gate pattern 26 is formed.
[0010] The size of a contact portion with the substrate of the above-mentioned T type gate pattern is determined with the opening size of the opening 25 of an insulator layer 21. In formation of a detailed pattern, the etching method has changed to dry etching from wet etching as a recent trend. therefore, Si O2 etc. -- if an insulator layer **********s, the side attachment wall of opening is formed in the almost perpendicular configuration However, a spacer is the thickness about 100nm - 200 nm, and does not become not much large [an aspect ratio]. Therefore, the step coverage when depositing gate metal is enough, and generating of a nest is not seen.
[0011] however, an etching of a detailed pattern sake -- CF4 required for dry etching NF3 etc. -- gas cannot go into opening easily, etching rates with a large pattern (for example, 1-micrometer level) differ, and it worries about damage by over etching

[Translation done.]

* NOTICES *

EFFECT OF THE INVENTION

[Effect of the Invention] it explained in full detail until now -- as -- this invention -- the photoresist film after development -- immediately -- or after forming a deterioration layer in a photoresist film front face, a reflow is carried out and the opening side attachment wall of a resist pattern is made to deform into a curve-like order taper This invention. In case an opening pattern is formed in an insulator layer etc., for example, the matter with which it **********s It presses down that a spatter is carried out to the side attachment wall of resist opening, and it becomes possible to prevent growth of the deterioration matter film which consists of mixture. Moreover, etching gas is sent as much as possible also into opening of a detailed pattern. It could ********** at the rate near the etching rate of a large pattern size, the step coverage at the time of depositing gate metal etc. on a resist pattern further was able to be improved, and the manufacture method of the semiconductor device which can prevent generating of a nest was able to be offered.

[Translation done.]

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] When using a resist as a mask and imprinting a detailed opening pattern to a ground insulator layer like the aforementioned 1st conventional example (refer to drawing 8 and drawing 9), a pattern size When it turns into 0.1-micrometer level grade minutely, the ground insulator layer matter with which it **********s carries out a spatter, and adheres to the side attachment wall of resist mask opening, the transformation matter film with which after resist mask removal consists of mixture remains, and excessive processing is needed in order to remove this. if it becomes a detailed size on the other hand -- etching gas -- opening -- entering -- hard -- becoming -- a pattern size -- for example, -- 1 micrometer and other large patterns differ from an etching rate, and there is a fear of receiving an injury.
[0013] Moreover, the technical problem that the step coverage of resist opening is bad like the aforementioned 2nd conventional example when forming T type gate pattern on a substrate by the lift-off method of a bilayer resist (refer to drawing 10), and a nest occurs in gate metal occurs.

[0014] Moreover, although it loses the technical problem of a step coverage in making an insulator into a spacer and forming T type gate pattern on a substrate by the lift-off method like the aforementioned 3rd conventional example (refer to drawing 11), by the size of a pattern size, etching rates differ, a large pattern serves as over etching, and there is a fear of receiving an injury.
[0015] It is what was made in order that this invention might solve the above-mentioned technical problem when imprinting a detailed pattern. the 1st purpose It presses down that the spatter of the matter with which it **********s is carried out to the side attachment wall of resist opening in case an opening pattern is formed in a ground insulator layer etc. It makes it possible to prevent growth of the transformation matter film which consists of mixture. the 2nd purpose Etching gas is sent as much as possible also into opening of a detailed pattern. It is offering the manufacture method of the semiconductor device which it makes it possible to ********** at the rate near the etching rate of a large pattern size, and the 3rd purpose's improves a step coverage at the time of deposition of gate metal etc., and can prevent generating of a nest.

[Translation done.]

MEANS

[Means for Solving the Problem] After the manufacture method of the semiconductor device concerning the claim 1 of this invention develops the photoresist film which exposed the pattern, it is characterized by including the process made to deform the opening side attachment wall of the aforementioned resist pattern into a curve-like order taper (that to which a resist side attachment wall has the tilt angle of 90 degrees or less in a ground layer principal plane) by heating and carrying out a reflow of this resist film.
[0017] Moreover, the manufacture method of the semiconductor device concerning the claim 2 of this invention is O2 to the photoresist film after the aforementioned development. After performing plasma treatment and forming a deterioration layer in this photoresist film front face, it is the manufacture method of a semiconductor device including the process made to deform the opening side attachment wall of the aforementioned resist pattern into a curve-like order taper according to claim 1 by heating and carrying out a reflow of this resist film.

[Translation done.]

OPERATION

[Function] Generally the resist after development performs a postbake, and a developer is evaporated or it is made to harden it to some extent by heating for the following process. however, by the manufacture method concerning the claim 1 of this invention If the postbake temperature of the resist pattern after development is raised to near the glass transition temperature of a resist higher than before A reflow starts and the rough edge of the character of the shoulder of opening is rounded off with an operation of surface tension. It moves in the direction in which it is roundish and the resist upper part spreads, and finally the size of a contact portion with a ground is not changed, but the opening upper part spreads, and an opening side attachment wall serves as a boiled-fish-paste-like order taper, and is stabilized (refer to drawing 1 (c)).
[0019] The insulator layer matter with which it will carry out the spatter of the boiled-fish-paste-like resist pattern by etching if such an opening side attachment wall **********s a ground insulator layer as for example, a mask for etching, and it adheres to an opening side attachment wall decreases in number sharply, the adhering transformation matter film is very thin, and it is O2 of the following process. It is completely removed with a resist by Usher. Moreover, in opening of such a configuration, sending of etching gas also becomes easy and the etching rate can make it the value near the etching rate of the opening pattern of a large size. Moreover, if the gate pattern by the lift-off method is formed by the resist pattern with opening of such a configuration, the step coverage in an opening shouldcr will improve sharply.
[0020] The manufacture method concerning the claim 2 of this invention is O2 to the resist pattern after development. Plasma is emitted, and after making it change to the matter which cannot solve the surface layer of a resist easily chemically, the same manufacture method as the above-mentioned claim 1 is applied.
[0021] detailed-izing -- progressing -- a pattern size -- for example, -- If it becomes thin below at 0.1-micrometer level, when a reflow of the resist film after development will be heated and carried out, opening may be closed conversely. By the manufacture method of a claim 2, the transformation layer which is hard to solve into a resist front face is formed, and it prevents that opening is closed. That is, the transformation layer of a resist film front face carries out the operation which prevents that the resist opening side attachment wall which counters carries out approach contact mutually by the reflow, and plugs up opening.

[Translation done.]

EXAMPLE

[Example] First, by heating and carrying out a reflow of the photoresist film after development explains the process made to deform the opening side attachment wall of a resist pattern into a curve-like order taper with reference to drawing 1 . This drawing (a) is Ga As. It is Si O2 on a substrate 3. It is the cross section which deposited the film 2 (less than [thickness 500nm]), and formed on it resist pattern (it may be called opening pattern or NUKIPA turn) 7a which has opening 4. Next, if a resist 1 is heated and it raises to near the glass transition temperature of a resist, a reflow will start. If a reflow starts as shown in this drawing (b), it will move in the direction in which the resist upper part spreads in opening 4 by operation of surface tension. Sign 7b expresses the resist pattern which began to spread. Finally, as shown in this drawing (c), the size of a contact portion with the ground layer 2 is not changed, namely, the size m of an opening pars basilaris ossis occipitalis is not changed, but it is [a side attachment wall forms the boiled-fish-paste-like curve 9, and] stable [size]. A sign 8 expresses a final resist pattern. This configuration It can form also with a pattern size with a level of 0.1 micrometers or less. It is presumed for force, such as a self-weight of the surface tension of the resist which the photoresist film 1 has been [the configuration] near a glass transition temperature in the state of a reflow, the statical friction force between this resist and a ground layer (boundary tension), and a resist film, to balance.
[0023] this invention is applied mainly to a detailed pattern imprint, and is considered that the thickness of thc ctched layer of a ground has an effect in etching of the thin film below 500 nm.
[0024] Moreover, Ga As At elements, such as a device, especially HEMT, it is Ga As constitutionally. About dozens of nm needs to ********** beforehand a part for the contact surface of a substrate and a gate electrode by recess etching. Since this process is needed and gate formation also forms gate metal by the lift off using a resist pattern, application of this invention is desirable.
[0025] Next, the 1st example which applied the claim 1 of this invention to the aforementioned 1st conventional example is explained with reference to drawing 2 and drawing 3 . it is shown in drawing 2 (a) -- as -- Ga As Si O2 deposited on the substrate 3 Or Si 3N4 etc. -- insulator layer 2 top Resist pattern 7a of 0.1-micrometer level is formed. At this example, it heat-treats at . resist development back which used PMMA (polymethylmethacrylate), and ZEP and Nippon Zeon for the resist 1, and the temperature of 100 degree C - 150 degrees C. A resist reflow begins, and heat-treatment is ended when a reflow is stable. As shown in drawing 2 (b), the resist pattern 8 which the side attachment wall transformed into the curve-like order taper 9 is obtained. Next, it is the ground insulator layer 2 CF4+H2 and CF4+O2 Using gas, as shown in drawing 3 (a), it **********ed by dry etching. They are after etching and a resist 1 O2 Ashing (remove a photoresist according to ashing in oxygen plasma) removes, as shown in drawing 3 (b). Although the resist pattern 8 had the curve-like order taper 9 in the above-mentioned example, in the ground thickness below 500 nm, the size conversion difference by the taper at the time of etching was not large. In addition, a size conversion difference is the width of face w1 of opening shown in drawing 2 (a), and the width of face w2 of the opening pars basilaris ossis occipitalis of the ground layer 2 shown in drawing 3 (b). It is a difference. Moreover, in order that a taper might attach a little the side attachment wall of the opening pattern 6 imprinted by the insulator layer 2, its coverage when depositing gate metal was also good.
[0026] in the above-mentioned example, although the opening side attachment wall of a resist pattern was made to deform into a curve-like order taper, a size conversion difference is also pressed down to the minimum, without the taper being imprinted by the ground film -- the opening pattern of 0.1micrometer level was able to be formed
[0027] It compares with the conventional technology, it is sharply thin, and the transformation matter film which grew up to be a resist opening side attachment wall by the spatter is O2 further on the occasion of the dry etching of the ground insulator layer 2 shown in drawing 3 (a). Since sputter etching is repeated and it is efficiently removed on the resist front face one by one with this resist configuration in ashing, it is O2. It became possible to remove the resist which contains a transformation matter film simply by ashing. Moreover, with the conventional technology of a perpendicular or a back taper configuration, although the opening side attachment wall of a resist pattern had produced the difference in the etching rate by the size of a pattern size, it was also able to make the difference small a little by using an opening side attachment wall as a curve-like order taper.
[0028] Next, the 2nd example (the lift-off method of a bilayer resist) which applied the claim 2 of this invention to the aforementioned 2nd conventional example is explained with reference to drawing 4 and drawing 5 . As shown in drawing 4 (a), it is Ga As about a positive resist 41. After using an application, a stepper, and an electron beam machine on a substrate 3 and drawing a pattern, negatives are developed and resist pattern 47a is formed. Next, O2 used for the usual resist ablation processing A plasma ashing device is used and it is O2 with about 50W] power. Flow rate 150 cc/min Processing is performed for 30 seconds, and as shown in this drawing (b), it is made the transformation layer 42 which cannot solve a resist surface layer easily chemically. 120 **-160 ** and 1 a part -2 a part -- a grade -- the substrate 3 was heated on the hot plate, a reflow of the photoresist 41 was carried out, and as shown in this drawing (c), the resist opening side attachment wall currently formed perpendicularly was formed in the order taper of about 60 degrees with 0 micrometer of size conversion differences at the base of opening [next,] A sign 48 expresses a lower layer resist pattern with this order taper side attachment wall 49. Next, as shown in drawing 5 (a), the upper resist pattern 46 of T type gate crowning is formed by the resist 43 without compatibility, and the gate metal 44 is deposited. As shown in this drawing (b), a resist is removed by the lift-off method and gate 44a is formed.
[0029] Since the curve-like order taper side attachment wall 49 is made to deform the side attachment wall of resist pattern 47a of the lower layer resist 41 of the 2nd example of the above as shown in drawing 4 (c), the step coverage of the gate metal 44 is good, and a nest does not generate it. Moreover, it is mitigated sharply, the phenomenon in which the side attachment wall which counters mutually [opening] to the resist pattern formation into which the opening size turned minutely more since a reflow is carried out after considering as the transformation layer 42 which cannot solve the photoresist surface layer after development into this example easily contacts, and a pattern is closed can also

form the order taper of about 60 degrees as mentioned above, and it is an opening pars-basilaris-ossis-occipitalis size in that case. It was less than ten percent of change.

[0030] Next, the 3rd example (the lift-off method which makes an insulator a spacer) which applied the claim 2 of this invention to the aforementioned 3rd conventional example is explained with reference to drawing 6 . it is shown in this drawing (a) -- as -- Ga As Si O2 which accumulates on a substrate 3 and serves as a spacer etc. -- the O2 [same after forming resist pattern 57a which consists of a positive resist 51 on an insulator layer 52] as the 2nd example of the above Plasma treatment is performed and the transformation layer 54 is formed in a resist film front face. Next, as shown in this drawing (b), an opening side attachment wall is used as the curve-like order taper side attachment wall 59 by heating and carrying out a reflow of the resist 51. Next, as shown in this drawing (c), the opening pattern 56 of an insulator layer is formed by processing an insulator layer 52 by dry etching, such as RIE, and removing a resist.

[0031] By this example, since it is a curve-like order taper side attachment wall, an etching rate becomes early and turns into an etching rate of a pattern with a large pattern size from the case where the side attachment wall of a resist pattern is the perpendicular former closely. That is, the difference of the etching rate by the size of a pattern size can be decreased. Moreover, by forming the transformation layer 54, it compares with the manufacture method concerning a claim 1, and a pattern size can also form a narrow pattern more, without closing opening.

[0032] In order to make the configuration of the opening side attachment wall of a resist pattern into an order taper configuration, there is also the method of light exposure being insufficient and exposing so that it may become thinner than a design size (refer to drawing 7).

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] In the manufacture method of the semiconductor device of this invention, it is the cross section showing the process which is made to carry out a reflow of the resist film, and deforms an opening side attachment wall into an order taper.
[Drawing 2] It is the cross section showing the manufacturing process of the 1st example of the manufacture method of the semiconductor device of this invention.
[Drawing 3] It is the cross section showing the manufacturing process following drawing 2 of the manufacture method of the semiconductor device of this invention.
[Drawing 4] It is the cross section showing the manufacturing process of the 2nd example of the manufacture method of the semiconductor device of this invention.
[Drawing 5] It is the cross section showing the manufacturing process following drawing 4 of the manufacture method of the semiconductor device of this invention.
[Drawing 6] It is the cross section showing the manufacturing process of the 3rd example of the manufacture method of the semiconductor device of this invention.
[Drawing 7] It is a cross section explaining the method of others which make the opening side attachment wall of a resist opening pattern an order taper configuration.
[Drawing 8] It is the cross section showing the manufacturing process of the 1st conventional example of the manufacture method of a semiconductor device.
[Drawing 9] It is the cross section showing the manufacturing process following drawing 8 of the 1st conventional example.
[Drawing 10] It is the cross section showing the manufacturing process of the 2nd conventional example of the manufacture method of a semiconductor device.
[Drawing 11] It is the cross section showing the manufacturing process of the 3rd conventional example of the manufacture method of a semiconductor device.
[Description of Notations]
1 Photoresist
2 Insulator Layer
3 Ga As Substrate
4 Opening
5 Transformation Matter Film
6 Opening Pattern of Insulator Layer
7a Resist pattern
8 Resist Pattern
9 Curve-like Order Taper (Side Attachment Wall)
41 Photoresist
42 Transformation Layer
44 Gate Metal
44a Gate pattern
47a Resist pattern
49 Curve-like Order Taper (Side Attachment Wall)
51 Photoresist
52 Insulator Layer
54 Transformation Layer
57a Resist pattern
59 Curve-like Order Taper (Side Attachment Wall)

[Translation done.]

* NOTICES *

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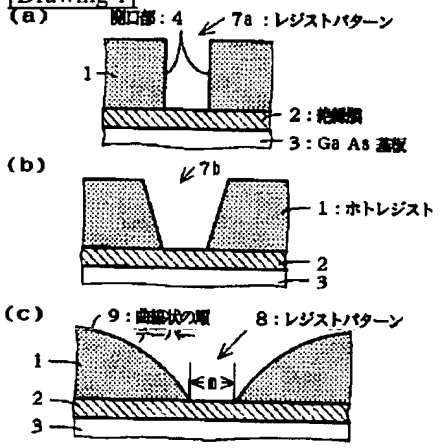
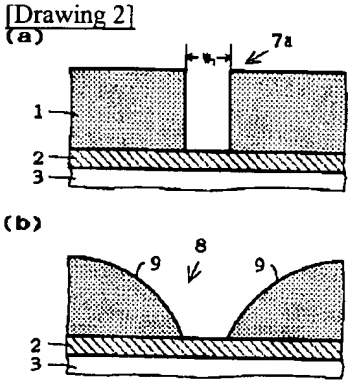
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

[Drawing 1]



[Drawing 2]



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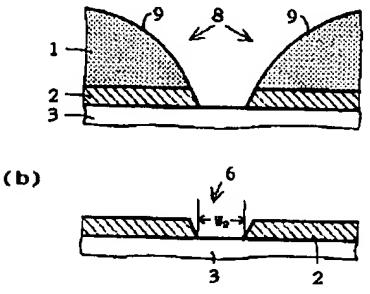

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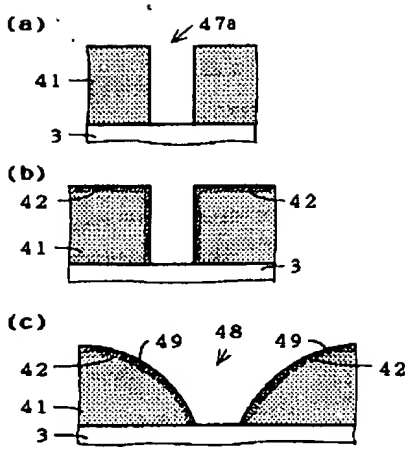

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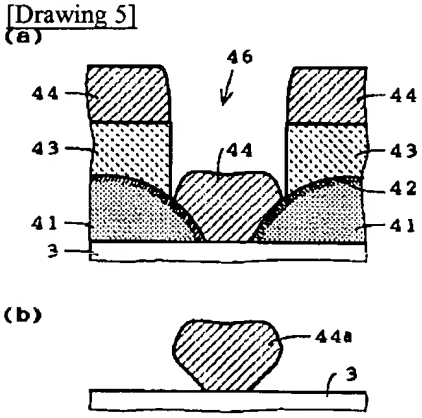
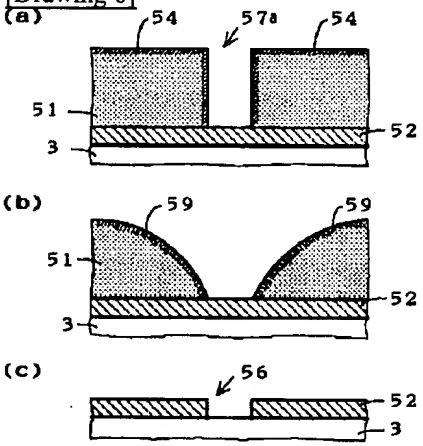
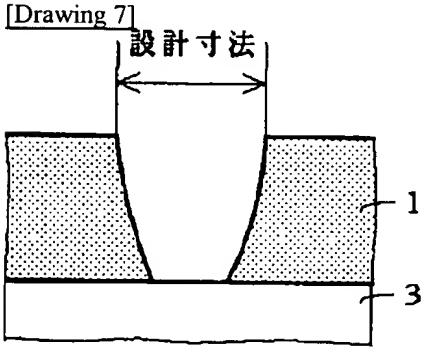


[Drawing 6]

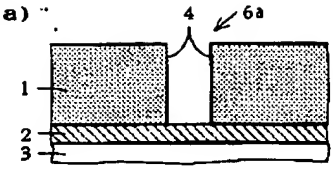


[Drawing 7]

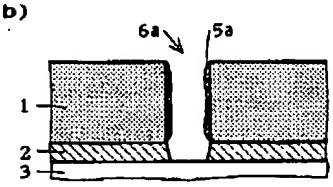


[Drawing 8]

(a)

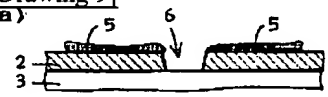


(b)



[Drawing 9]

(a)



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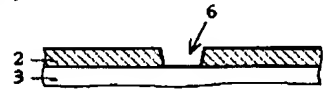
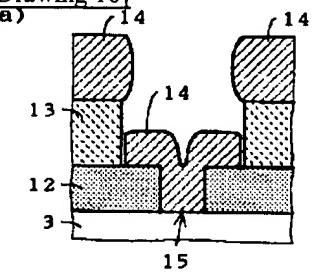


[Drawing 10]

(a)



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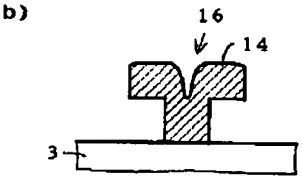
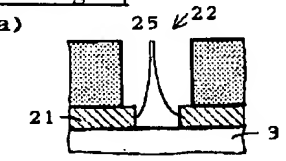


[Drawing 11]

(a)



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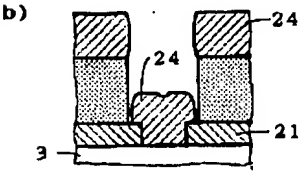
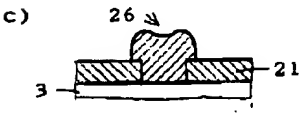


(c)



[Translation done.]

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		7352－4M	Ｈ０１Ｌ　21/ 30　３６１　Ｑ	

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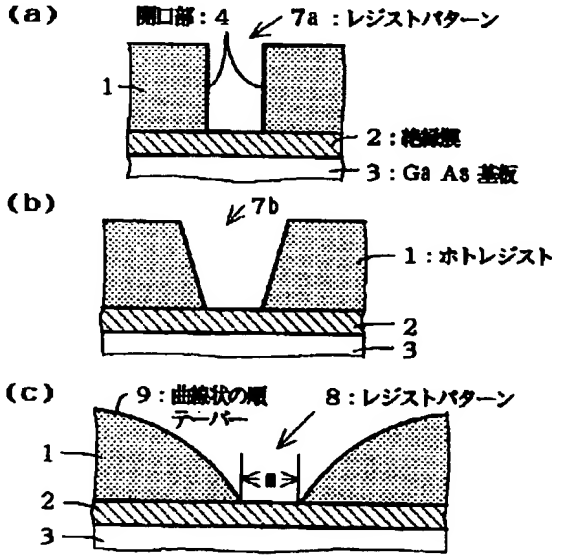
(54)【発明の名称】　半導体装置の製造方法

(57)【要約】
【目的】0.1μｍレベルの微細パターンを転写するとき、（イ）例えばレジストをマスクとして絶縁膜に開口パターンを形成する際、エッチングされる物質がレジスト開口部の側壁にスパッタし、レジスト除去後も変質物質膜として残ったり、（ロ）パターン寸法の大小によってエッチングレートが異なったり、（ハ）リフトオフ法によるゲートパターンなどを形成するときステップカバレージが悪いことなどの課題を解決する。
【構成】現像後直ちに、または現像後ホトレジスト膜にO_2 プラズマ処理を行ない表面に変質層を形成した後、レジスト膜を加熱してリフローさせ、レジストパターンの開口部側壁を曲線状の順テーパーに変形させることにより、目的を達成できる。



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【特許請求の範囲】

【請求項1】パターンを露光したホトレジスト膜を現像した後、該レジスト膜を加熱してリフローさせることにより前記レジストパターンの開口部側壁を曲線状の順テーパーに変形させる工程を含むことを特徴とする半導体装置の製造方法。

【請求項2】前記現像後のホトレジスト膜に、O_2 プラズマ処理を行ない該ホトレジスト膜表面に変質層を形成した後、該レジスト膜を加熱してリフローさせることにより前記レジストパターンの開口部側壁を曲線状の順テーパーに変形させる工程を含む請求項1記載の半導体装置の製造方法。

【発明の詳細な説明】

【0001】

【産業上の利用分野】本発明は、半導体装置の製造方法に関するもので、特にリソグラフィー技術における微細パターンを転写するためのレジストパターンの形成に使用される。

【0002】

【従来の技術】微細パターンを転写する第1の従来例として、半導体基板上に形成された絶縁膜にレジストをマスクとし微細な開口パターンを転写する工程を例にとり説明する。

【0003】従来、レジストなどをマスクにして絶縁膜をドライエッチングしてパターンを転写する場合には、マスクとなるレジストの開口部幅寸法は、設計値に近い寸法で、かつほぼ側壁が垂直か、若干テーパーを成しているものが理想的であり、そのレジストパターン（レジスト上に開口溝で描いた図形、または図形が描かれたレジスト膜）を使い、目的の下地絶縁膜をエッチングしている。図8及び図9は、レジストパターニングを行ない、下地絶縁膜をエッチングするときの従来の製造工程を示す断面図である。

【0004】図8（a）は、Ga As 基板3に形成された$Si\ O_2$ またはSi_3N_4 等の絶縁膜2上に、レジスト1を塗布し、開口部4を持つ 0.1μmレベルの開口パターン（ヌキパターンとも呼び開口溝で描かれた図形）6aを形成した図である。サブミクロンからさらに超微細化した 0.1μm以下の寸法レベルにおいては、現状では電子ビームを使用し、レジストパターニングを行なっている。この場合、現像後のレジストパターンの開口部側壁は、垂直、もしくは電子ビームのバックスキッタの影響を受けて逆テーパー形状となる。次に同図（b）において、上記形状のレジストパターンを用い、下地層（$Si\ O_2$ 膜など）2を（CF_4 ＋O_2 ）／（CF_4 ＋H_2 ）などでエッチングすると、側壁がほぼ垂直に切り立った加工が可能である。しかし、この場合開口部の幅が狭いため、通常のドライエッチングでは効率良くエッチングされ飛び散る（スパッタ）べき物質5aが、どうしても開口部側壁に付着してしまう。そのため本来のエッチングが終了した後、レジストをO_2 アッシャーなどで剥離した場合、図9（a）に示すように、薄い膜状のレジストとエッチングされた物質、さらにエッチングガス材の混合物からなる変質物質膜5が残ってしまう。なお符号6は、絶縁膜2に転写された開口パターンである。このため同図（b）に示すように、例えばフッ化アンモニウムで変質物質膜5を除去するウェット処理などの追加を必要とする。

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【0005】他方、素子のデザインにより、一般的にパターンの開口部の幅寸法（以下単にパターン寸法と記す）は大小様々なものが混在している。パターン寸法が細いほどエッチングガスは入りにくいため、エッチングレートが遅くなってしまう。そのため 0.1μmと 1μm程度の寸法差のパターンが混在しているとエッチングレートが異なり、例えば 0.1μm領域のエッチング量を適正値とすると、 1μm領域ではオーバーエッチングされてしまう。

【0006】次に微細パターンを転写する第2の従来例として、Ga As デバイス（HEMTなど）で用いられているT型（マッシュルーム型）ゲートパターンを形成する例について説明する。図10は従来の二層レジスト法によるT型ゲートパターンの製造工程を示す断面図である。同図（a）において、Ga As 基板3上に開口パターン15（例えばパターン寸法 0.2μm）を有する下層レジスト膜12を形成し、次に相溶性の無いレジストによりT型ゲートパターン頂部の上層レジスト膜13を形成し、ゲートメタル14を堆積する。次にリフトオフ法によりレジストを除去し、同図（b）に示すようにT型ゲートパターン16を形成する。

【0007】二層レジスト・プロセス法については、下層レジスト膜12で形成された開口パターン15のパターン寸法により、ゲート長が決定される。そのため開口パターン15としては開口部の幅寸法の精度が良く、さらに開口部のレジスト側壁が垂直であるものが望ましい。

【0008】しかしし開口パターン15が上記形状では、次の工程でゲートメタルを堆積した際、ステップカバレージ（step coverage 、LSI等の半導体素子薄膜の表面における微細な段差部での膜の被着状態のこと）が悪くなるなどの原因から、ゲートメタル内に巣が発生しやすくなる。

【0009】次に微細パターンを転写する第3の従来例として、前記T型ゲートパターンを別の従来技術、すなわち絶縁膜をスペーサーとするT型ゲートパターンの形成方法について説明する。図11は、この製造工程を示す断面図である。同図（a）において、Ga As 基板3上にスペーサーとなる厚さ100 nm～200 nmの$Si\ O_2$ 等の絶縁膜21を堆積し、その上にレジストパターン22を形成し、次に絶縁膜21をドライエッチングして開口部25を形成する。次に同図（b）に示すように、ゲー

トメタル24を堆積し、次に同図（c）に示すように、リフトオフ法にてレジストを除去し、T型ゲートパターン26を形成する。

【0010】上記T型ゲートパターンの基板との接触部分の寸法は絶縁膜21の開口部25の開口寸法で決定される。微細パターンの形成では、最近の傾向として、ウェットエッチングからドライエッチングにエッチング方法が変わっている。そのため、SiO_2 などの絶縁膜がエッチングされると、開口部の側壁は、ほぼ垂直な形状で形成されている。しかしスペーサーは100nm～200 nm程度の厚さであり、アスペクト比もあまり大きくならない。そのためゲートメタルを堆積したときのステップカバレージは十分であり巣の発生は見られない。

【0011】しかし微細パターンのエッチングのため、ドライエッチングに必要なCF_4 やNF_3 等のガスが開口部に入りにくく、大きいパターン（例えば 1μmレベル）とのエッチングレートが異なってしまい、オーバーエッチングによる損傷が心配される。

【0012】

【発明が解決しようとする課題】前記第1従来例のように、レジストをマスクにして、下地絶縁膜に微細な開口パターンを転写する場合（図8、図9参照）、パターン寸法が 0.1μmレベル程度に微細化されると、エッチングされる下地絶縁膜物質がスパッタしてレジストマスク開口部の側壁に付着し、レジストマスク除去後も混合物からなる変質物質膜が残り、これを除去するため余分の処理を必要とする。一方微細寸法になるとエッチングガスが開口部に入りにくくなって、パターン寸法が例えば 1μmと大きい他のパターンとエッチングレートが異なり、損傷を受ける心配がある。

【0013】また前記第2従来例のように、二層レジストのリフトオフ法により基板上にT型ゲートパターンを形成する場合（図10参照）レジスト開口部のステップカバレージが悪く、ゲートメタル内に巣が発生するという課題がある。

【0014】また前記第3従来例のように、絶縁物をスペーサーとし、リフトオフ法により基板上にT型ゲートパターンを形成する場合（図11参照）には、ステップカバレージの課題はなくなるが、パターン寸法の大小により、エッチングレートが異なり、大きいパターンがオーバーエッチングとなり、損傷を受ける心配がある。

【0015】本発明は、微細パターンを転写するときの上記課題を解決するためになされたもので、第1の目的は、下地絶縁膜などに開口パターンを形成する際、エッチングされる物質がレジスト開口部の側壁にスパッタされるのを押さえ、混合物から成る変質物質膜の成長を防ぐことを可能とし、第2の目的は、微細パターンの開口部にも、できるだけエッチングガスを送り込み、大きいパターン寸法のエッチングレートに近いレートでエッチングすることを可能とし、第3の目的はゲートメタルなどの堆積時にステップカバレージを良くし、巣の発生を防止できる半導体装置の製造方法を提供することである。

【0016】

【課題を解決するための手段】本発明の請求項1に係る半導体装置の製造方法は、パターンを露光したホトレジスト膜を現像した後、該レジスト膜を加熱してリフローさせることにより前記レジストパターンの開口部側壁を曲線状の順テーパー（レジスト側壁が下地層主面に90°以下の傾斜角を持つもの）に変形させる工程を含むことを特徴とするものである。

【0017】また本発明の請求項2に係る半導体装置の製造方法は、前記現像後のホトレジスト膜に、O_2 プラズマ処理を行ない該ホトレジスト膜表面に変質層を形成した後、該レジスト膜を加熱してリフローさせることにより前記レジストパターンの開口部側壁を曲線状の順テーパーに変形させる工程を含む請求項1記載の半導体装置の製造方法である。

【0018】

【作用】現像後のレジストは、一般的にポストベークを行ない、現像液を蒸発させたり、次工程のため、加熱によりある程度硬化させる。しかし本発明の請求項1に係る製造方法では、現像後のレジストパターンのポストベーク温度を従来より高いレジストのガラス転移温度付近まで上げると、リフローが始まり、表面張力の作用により開口部の肩口は角がとれ、丸みをおびレジスト上部が広がる方向に移動し、最終的には下地との接触部分の寸法は変動せず、開口部上部は広がり、開口部側壁は、カマボコ状の順テーパーとなり、安定化する（図1（c）参照）。

【0019】このような開口部側壁がカマボコ状のレジストパターンを、例えばエッチング用マスクとして下地絶縁膜をエッチングすれば、エッチングによりスパッタして開口部側壁に付着する絶縁膜物質は大幅に減少し、その付着する変質物質膜は極めて薄く、次工程のO_2 アッシャーにより、レジストと共に完全に除去される。またこのような形状の開口部では、エッチングガスの送り込みも容易となり、そのエッチングレートは大きい寸法の開口パターンのエッチングレートに近い値とすることができる。またこのような形状の開口部を持つレジストパターンで、リフトオフ法によるゲートパターンを形成すると、開口部肩部におけるステップカバレージは大幅に改善される。

【0020】本発明の請求項2に係る製造方法は、現像後のレジストパターンに対し、O_2 プラズマを放射し、レジストの表面層を化学的にとけにくい物質に変化させた後、上記請求項1と同様の製造方法を適用するものである。

【0021】微細化が進み、パターン寸法が例えば 0.1μmレベル以下に細くなると、現像後のレジスト膜を加

熱してリフローさせると、逆に開口部が塞がってしまうことがある。請求項2の製造方法ではレジスト表面にとけにくい変質層を形成し、開口部が塞がるのを防止する。すなわちレジスト膜表面の変質層は、対向するレジスト開口部側壁がリフローにより互いに接近接触して開口部を塞ぐのを防止する作用をする。

【0022】

【実施例】まず、現像後のホトレジスト膜を加熱してリフローさせることにより、レジストパターンの開口部側壁を曲線状の順テーパーに変形させる工程について、図1を参照して説明する。同図（a）は、Ga As 基板3上にSi O_2 膜2（膜厚 500nm以下）を堆積し、その上に開口部4を有するレジストパターン（開口パターンまたはヌキパターンと呼ぶこともある）7aを形成した断面図である。次にレジスト1を加熱して、レジストのガラス転移温度の付近まで上げるとリフローが始まる。同図（b）に示すように、リフローが始まると表面張力の作用により開口部4ではレジスト上部が広がる方向に移動する。符号7bは広がり始めたレジストパターンを表わす。最終的には、同図（c）に示すように、下地層2との接触部分の寸法は変動せず、すなわち開口底部の寸法mは変動せず、側壁がカマボコ状の曲線9を形成して安定化する。符号8は最終的なレジストパターンを表わす。この形状は 0.1μm以下のレベルのパターン寸法でも形成可能である。ホトレジスト膜1が、リフローの状態で、その形状が安定化するのは、ガラス転移温度付近にあるレジストの表面張力、該レジストと下地層との間の静摩擦力（界面張力）及びレジスト膜の自重等の力がバランスするためと推定される。

【0023】本発明は、主として微細なパターン転写に適用されるものであり、例えば下地の被エッチング層の膜厚が500 nm以下の薄膜のエッチングに効果があると考えられる。

【0024】またGa As デバイス、特にHEMTなどの素子では、構成上、Ga As 基板とゲート電極の接点部分を、リセスエッチングにより、あらかじめ数十nm程度エッチングする必要がある。この工程を必要とするため、ゲート形成もレジストパターンを使いゲートメタルをリフトオフで形成しているので、本発明の適用が望ましい。

【0025】次に前記第1従来例に、本発明の請求項1を適用した第1の実施例について図2及び図3を参照して説明する。図2（a）に示すように、Ga As 基板3上に堆積したSi O_2 またはSi $_3N_4$ 等の絶縁膜2上に 0.1μmレベルのレジストパターン7aを形成する。本実施例では、レジスト1にPMMA（ポリメチルメタクリレート）やZEP・日本ゼオンを用いた．レジスト現像後、 100℃～150℃の温度で加熱処理する。レジストリフローが開始し、リフローが安定化した時点で加熱処理を終了する。図2（b）に示すように、側壁が曲線

状の順テーパー9に変形したレジストパターン8が得られる。次に下地絶縁膜2をCF_4 ＋H_2 、CF_4 ＋O_2 ガスを用いて、図3（a）に示すように、ドライエッチングによりエッチングした。エッチング後、レジスト1を、O_2 アッシング（酸素プラズマ中でホトレジストを灰化により除去すること）により、図3（b）に示すように除去する。　上記実施例で、レジストパターン8は、曲線状の順テーパー9を有していたが、500 nm以下の下地膜厚では、エッチング時のテーパーによる寸法変換差は、大きくなかった。なお寸法変換差は図2（a）に示す開口部の幅w_1と、図3（b）に示す下地層2の開口底部の幅w_2 との差である。また絶縁膜2に転写された開口パターン6の側壁は、若干テーパーがつくため、ゲートメタルを堆積したときのカバレージも良かった。

【0026】上記実施例では、レジストパターンの開口部側壁を曲線状の順テーパーに変形させたが、そのテーパーが下地膜に転写されることなく、寸法変換差も最小限に押さえられ、 0.1μmレベルの開口パターンを形成することができた。

【0027】図3（a）に示す下地絶縁膜2のドライエッチングに際し、スパッタによりレジスト開口側壁に成長した変質物質膜は、従来技術に比し大幅に薄く、さらにO_2 アッシングでは、今回のレジスト形状により、順次レジスト表面でスパッタエッチングを繰り返し、効率的に除去されているため、O_2 アッシングにより、簡単に変質物質膜を含むレジストを除去することが可能となった。またレジストパターンの開口側壁が垂直や逆テーパー形状の従来技術では、パターン寸法の大小によりエッチングレートに差を生じていたが、開口側壁を曲線状の順テーパーとすることにより、その差も若干小さくすることができた。

【0028】次に前記第2従来例に、本発明の請求項2を適用した第2の実施例（二層レジストのリフトオフ法）について図4及び図5を参照して説明する。図4（a）に示すように、ポジ型レジスト41をGa As 基板3上に塗布、ステッパーや電子ビーム露光装置を用いて、パターンを描画した後、現像してレジストパターン47aを形成する。次に通常のレジスト剥離処理に用いるO_2 プラズマアッシング装置を使い、50W程度の電力にて、O_2 流量150 cc／min で30秒間処理を行ない、同図（b）に示すように、レジスト表面層を化学的にとけにくい変質層42にする。次に、120 ℃～160 ℃、1 分～2 分程度、加熱板上で基板3を加熱し、ホトレジスト41をリフローさせ、同図（c）に示すように、垂直に形成されていたレジスト開口側壁を、開口底面の寸法変換差0μmにて約60度の順テーパーに形成した。符号48は、この順テーパー側壁49を持つ下層レジストパターンを表わす。次に図5（a）に示すように、相溶性のないレジスト43にてT型ゲート頂部の上層レジストパ

ターン４６を形成し、ゲートメタル４４を堆積する。同図（ｂ）に示すように、リフトオフ法にてレジストを除去し、ゲート４４ａを形成する。

【００２９】上記第２実施例の下層レジスト４１のレジストパターン４７ａの側壁は、図４（ｃ）に示すように、曲線状の順テーパー側壁４９に変形させられているので、ゲートメタル４４のステップカバレージは良く、巣の発生することもない。また本実施例では、現像後のホトレジスト表面層をとけにくい変質層４２とした後、リフローさせるので、開口寸法がより微細化されたレジストパターン形成に対し、開口部の互いに対向する側壁が接触してパターンが塞がってしまう現象も大幅に軽減され、上記のようにほぼ60度の順テーパーを形成でき、その際の開口底部寸法は 1割以内の変動であった。

【００３０】次に前記第３従来例に本発明の請求項２を適用した第３の実施例（絶縁物をスペーサーとするリフトオフ法）について図６を参照して説明する。同図（ａ）に示すように、Ga As 基板３上に堆積されスペーサーとなるSi O_2 等の絶縁膜５２上に、ポジ型レジスト５１から成るレジストパターン５７ａを形成した後、前記第２実施例と同様のO_2 プラズマ処理を行ないレジスト膜表面に変質層５４を形成する。次に同図（ｂ）に示すように、レジスト５１を加熱してリフローさせることにより、開口部側壁を曲線状の順テーパー側壁５９にする。次に同図（ｃ）に示すように、絶縁膜５２をＲＩＥなどのドライエッチングにより加工し、レジストを除去することにより、絶縁膜の開口パターン５６を形成する。

【００３１】レジストパターンの側壁が垂直である従来の場合より、本実施例では、曲線状の順テーパー側壁となっているので、エッチングレートは早くなり、パターン寸法の大きいパターンのエッチングレートに近くなる。すなわちパターン寸法の大小によるエッチングレートの差を減少させることができる。また変質層５４を形成することにより、請求項１に係る製造方法に比し、パターン寸法がより細いパターンでも開口部が塞がることなく形成できる。

【００３２】レジストパターンの開口部側壁の形状を順テーパー形状にするためには、設計寸法より細くなるように、露光量不足で露光する方法もある（図７参照）。

【００３３】

【発明の効果】これまで詳述したように、本発明では現像後のホトレジスト膜を直ちに、またはホトレジスト膜表面に変質層を形成した後、リフローさせてレジストパターンの開口部側壁を曲線状の順テーパーに変形させる。この発明により、例えば絶縁膜などに開口パターンを形成する際、エッチングされる物質が、レジスト開口部の側壁にスパッタされるのを押さえ、混合物から成る変質物質膜の成長を防ぐことが可能となり、また微細パターンの開口部にも、できるだけエッチングガスを送り込み、大きいパターン寸法のエッチングレートに近いレートでエッチングすることができ、さらにレジストパターンにゲートメタルなどを堆積する際のステップカバレージを良くし、巣の発生を防止できる半導体装置の製造方法を提供することができた。

【図面の簡単な説明】

【図１】本発明の半導体装置の製造方法において、レジスト膜をリフローさせ開口部側壁を順テーパーに変形する工程を示す断面図である。

【図２】本発明の半導体装置の製造方法の第１実施例の製造工程を示す断面図である。

【図３】本発明の半導体装置の製造方法の図２に続く製造工程を示す断面図である。

【図４】本発明の半導体装置の製造方法の第２実施例の製造工程を示す断面図である。

【図５】本発明の半導体装置の製造方法の図４に続く製造工程を示す断面図である。

【図６】本発明の半導体装置の製造方法の第３実施例の製造工程を示す断面図である。

【図７】レジスト開口パターンの開口部側壁を順テーパー形状にするその他の方法を説明する断面図である。

【図８】半導体装置の製造方法の第１の従来例の製造工程を示す断面図である。

【図９】第１の従来例の図８に続く製造工程を示す断面図である。

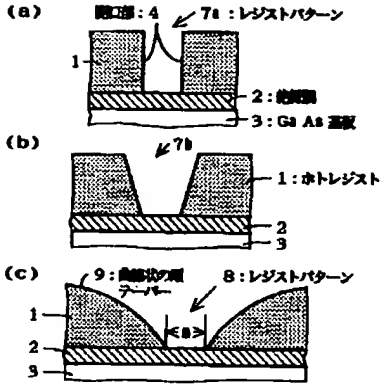
【図１０】半導体装置の製造方法の第２の従来例の製造工程を示す断面図である。

【図１１】半導体装置の製造方法の第３の従来例の製造工程を示す断面図である。

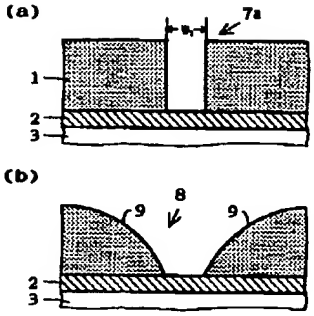
【符号の説明】

１　ホトレジスト
２　絶縁膜
３　Ga As 基板
４　開口部
５　変質物質膜
６　絶縁膜の開口パターン
７ａ　レジストパターン
８　レジストパターン
９　曲線状の順テーパー（側壁）
４１　ホトレジスト
４２　変質層
４４　ゲートメタル
４４ａ　ゲートパターン
４７ａ　レジストパターン
４９　曲線状の順テーパー（側壁）
５１　ホトレジスト
５２　絶縁膜
５４　変質層
５７ａ　レジストパターン
５９　曲線状の順テーパー（側壁）

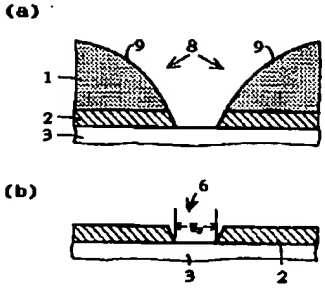
【図1】



【図2】



【図3】



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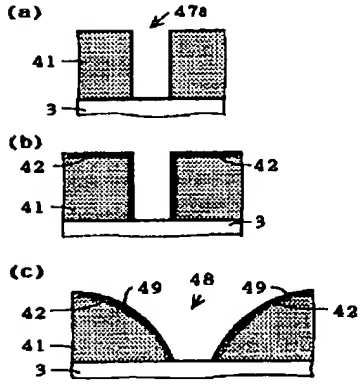

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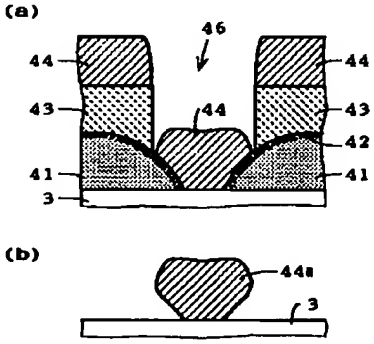

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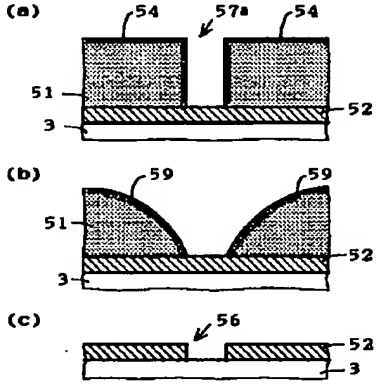
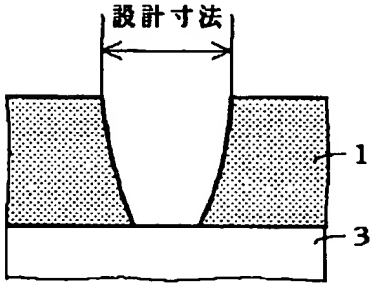


【図7】



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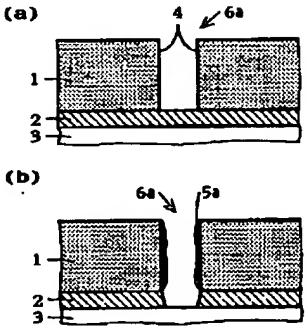
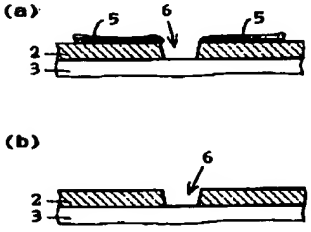
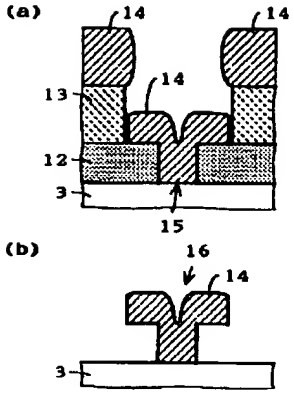


【図9】



【図10】



【図11】